

**Digital Logic Lab Assignment # 1**

**1.** To verify the basic operation of logic gates.

# Submitted By

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**Year/SEM : 2017/1st Semester**

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# Submitted To

|  |  |  |
| --- | --- | --- |
|  | **Signature** | **Remarks** |
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**OBJECTIVE 1.1:**

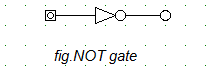
**TO VERIFY THE OPERATION OF NOT GATE.**

**THEORY:**

**NOT gate** is a [logic gate](https://en.wikipedia.org/wiki/Logic_gate) which implements [logical negation](https://en.wikipedia.org/wiki/Logical_negation). If the applied input is low then the output becomes high and vice versa.

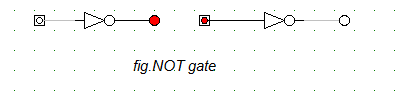
**Boolean expression’s= A’**

**CIRCUIT DIAGRAM:**

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**TRUTH TABLE:**

|  |  |
| --- | --- |
| **INPUT** | **OUTPUT** |
| **A** | **A’** |
| **0** | **1** |
| **1** | **0** |

**OBSERVATION: **

**OBSERVATION TABLE:**

|  |  |
| --- | --- |
| **INPUT** | **OUTPUT** |
| **A** | **A’** |
| **0** | **1** |
| **1** | **0** |

**CONCLUSION:**

Hence, the logical operation of NOT gate was verified.

**REFERENCE:** <http://www.physicshandbook.com/topic/topicc/combgates.htm>

**OBJECTIVE 1.2:**

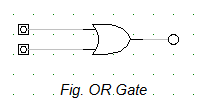
**TO VERIFY OPERATION OF OR GATE.**

**THEORY:**

**The OR gate is a digital**[**logic gate**](https://en.wikipedia.org/wiki/Logic_gate)**that implements**[**logical disjunction**](https://en.wikipedia.org/wiki/Logical_disjunction)**.** **A HIGH output (1) results if one or both the inputs to the gate are HIGH (1). If neither input is high, a LOW output (0) results.**

**Boolean expression: F= (A+B)**

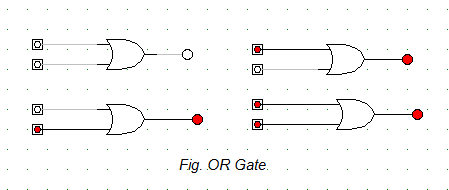
**CIRCUIT DIAGRAM:**

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**TRUTH TABLE:**

|  |  |  |
| --- | --- | --- |
| **INP** | **UTS** | **OUTPUT** |
| **A** | **B** | **(A+B)** |
| **0** | **0** | **0** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **1** |

**OBSERVATION:**

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**OBSERVATION TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **INP** | **UTS** | **OUTPUT** |
| **A** |  | **B** | **(A+B)** |
| **0** |  | **0** | **0** |
| **0** |  | **1** | **1** |
| **1** |  | **0** | **1** |
| **1** |  | **1** | **1** |

**CONCLUSION:**

Hence, the property of OR gate was verified.

**REFERENCE:**

http://www.physicshandbook.com/topic/topicc/combgates.htm

**OBJECTIVE 1.3:**

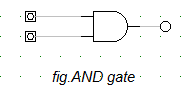
**TO VERIFY OPERATION OF AND GATE.**

**THEORY:**

**The AND gate is a basic digital**[**logic gate**](https://en.wikipedia.org/wiki/Logic_gate)**that implements**[**logical conjunction**](https://en.wikipedia.org/wiki/Logical_conjunction)**.** **A HIGH output (1) results only if both the inputs to the AND gate are HIGH (1). If neither or only one input to the AND gate is HIGH, a LOW output results**

**Boolean expression: F= (A.B)**

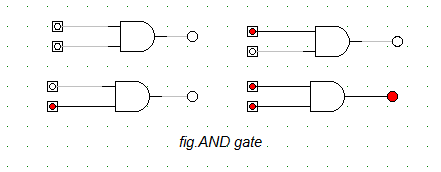
**CIRCUIT DIAGRAM:**

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**TRUTH TABLE:**

|  |  |  |
| --- | --- | --- |
| **INP** | **UTS** | **OUTPUT** |
| **A** | **B** | **(A.B)** |
| **0** | **0** | **0** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **1** |

**OBSERVATION:**

****

**OBSERVATION TABLE:**

|  |  |  |  |
| --- | --- | --- | --- |
|  | **INP** | **UTS** | **OUTPUT** |
| **A** |  | **B** | **(A.B)’** |
| **0** |  | **0** | **0** |
| **0** |  | **1** | **0** |
| **1** |  | **0** | **0** |
| **1** |  | **1** | **1** |

**CONCLUSION:**

Hence, the property of AND gate was verified.

**REFERENCE:**

**http://www.physicshandbook.com/topic/topicc/combgates.htm**